

Appl. No. 10/734,928
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Reply to Office Action of 02/04/2005

IN THE CLAIMS

Please amend claims 43 and 47 as follows below.

Please cancel claim 48 without prejudice.

The following is a listing of claims that replaces all prior versions, and listings, of claims in the application:

Listing of Marked Up Claims:

1 1- 22. (Cancelled).

1 23. (Previously Presented) A bipolar transistor,
2 comprising:
3 a substrate to provide a collector region;
4 a base region having an intrinsic base region and an
5 extrinsic base region, each of the intrinsic base region and
6 the extrinsic base region having a mono-crystalline portion
7 over a mono-crystalline portion of the substrate; and
8 an emitter structure over the intrinsic base region;
9 wherein the extrinsic base region is raised relative to
10 the intrinsic base region;
11 wherein the extrinsic base region has a thickness x and
12 the intrinsic base region has a thickness y , and wherein x
13 is greater than y .

1 24. (Previously Presented) The bipolar transistor of
2 claim 23, wherein
3 the emitter structure includes

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4 a polysilicon emitter having a first portion with
5 a width a , a second portion with a width b , and a third
6 portion with a width c ;
7 wherein c is greater than b which is greater than
8 a ; and
9 wherein the first portion defines an emitter base
10 junction, and wherein the third portion defines an
11 emitter contact region.

1 25. (Previously Presented) The bipolar transistor of
2 claim 24, wherein
3 the emitter structure further includes a nitride spacer
4 directly adjacent to the polysilicon emitter.

1 26. (Original) The bipolar transistor of claim 23,
2 wherein
3 the extrinsic base region comprises:
4 a first epitaxial layer; and
5 a second epitaxial layer on the first epitaxial
6 layer.

1 27. (Previously Presented) The bipolar transistor of
2 claim 26, wherein
3 the first epitaxial layer is a SiGe epitaxial layer and
4 the second epitaxial layer is a heavily p-type doped Si
5 or SiGe epitaxial layer.

1 28. (Previously Presented) The bipolar transistor of
2 claim 23, wherein

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3 the bipolar transistor is an npn transistor.

1 29. (Previously Presented) A bipolar transistor,
2 comprising:

3 a substrate having a collector region, the collector
4 region being a collector terminal;

5 a first epitaxial silicon layer having a mono-
6 crystalline portion on a mono-crystalline portion of the
7 substrate;

8 an emitter stack on the first epitaxial silicon layer,
9 the emitter stack being an emitter terminal;

10 a second epitaxial silicon layer having a mono-
11 crystalline portion on the mono-crystalline portion of the
12 first epitaxial silicon layer located outside the emitter
13 stack;

14 wherein a region of the first epitaxial silicon layer
15 located under the emitter stack is an intrinsic base region
16 and a region of the second epitaxial silicon layer on
17 portions of the first epitaxial silicon layer located
18 outside the emitter stack being a raised extrinsic base
19 region;

20 wherein the raised extrinsic base region has a
21 thickness greater than a thickness of the intrinsic base
22 region; and

23 wherein the intrinsic base region and the raised
24 extrinsic base region provide a base terminal of the bipolar
25 transistor with lower resistivity.

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1 30. (Previously Presented) The bipolar transistor of
2 claim 29, wherein

3 the first epitaxial layer is a p-type Si, SiGe or
4 SiGe:C epitaxial layer and

5 the second epitaxial layer is a selectively deposited
6 heavily p-type doped Si epitaxial layer or a selectively
7 deposited heavily p-type doped SiGe epitaxial layer.

1 31. (Previously Presented) The bipolar transistor of
2 claim 29, wherein

3 the emitter stack includes

4 a nitride layer having an emitter window, and
5 a polysilicon emitter within the emitter window.

1 32. (Previously Presented) The bipolar transistor of
2 claim 29, wherein

3 the bipolar transistor is a Si, SiGe or SiGe:C npn
4 bipolar transistor.

1 33. (Previously Presented) A bipolar transistor
2 having a base, a collector, and an emitter, the bipolar
3 transistor comprising:

4 a substrate with a collector region;

5 a base region coupled to the substrate, the base region
6 having an intrinsic base region and an extrinsic base
7 region, each of the intrinsic base region and the extrinsic
8 base region having a mono-crystalline portion over a mono-
9 crystalline portion of the substrate;

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10 a polysilicon emitter structure coupled to the
11 intrinsic base region; and
12 wherein the extrinsic base region has a thickness X and
13 the intrinsic base region has a thickness y, and wherein X
14 is greater than Y.

1 34. (Previously Presented) The bipolar transistor of
2 claim 33, wherein
3 the extrinsic base region is raised relative to the
4 intrinsic base region.

1 35. (Previously Presented) The bipolar transistor of
2 claim 33, wherein
3 the polysilicon emitter structure has a first portion
4 providing an emitter base junction, a second portion
5 providing conduction, and a third portion providing an
6 emitter contact region.

1 36. (Previously Presented) The bipolar transistor of
2 claim 35, wherein
3 the first portion of the polysilicon emitter structure
4 has a width A,
5 the second portion of the polysilicon emitter structure
6 has a width B differing from A,
7 the third portion of the polysilicon emitter structure
8 has a width C differing from A and C.

1 37. (Previously Presented) The bipolar transistor of
2 claim 36, wherein

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3 the width C is greater than the width B which is
4 greater than the width A.

1 38. (Previously Presented) The bipolar transistor of
2 claim 23, wherein

3 the extrinsic base region further has a poly-
4 crystalline portion over an oxide layer of the substrate.

1 39. (Previously Presented) The bipolar transistor of
2 claim 23, further comprising:

3 a silicide layer on a top surface of the extrinsic base
4 region to lower a contact resistance.

1 40. (Previously Presented) The bipolar transistor of
2 claim 39, wherein

3 the silicide layer is a refractory metal silicide layer
4 of CoSi_2 or TiSi_2 .

1 41. (Previously Presented) The bipolar transistor of
2 claim 29, wherein

3 the first epitaxial layer further has a poly-
4 crystalline portion on an oxide layer of the substrate, and

5 the second epitaxial layer further has a has a poly-
6 crystalline portion on the poly-crystalline portion of the
7 first epitaxial layer.

1 42. (Previously Presented) The bipolar transistor of
2 claim 29, further comprising:

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3 a silicide layer on a top surface of the second
4 epitaxial silicon layer to lower a contact resistance.

1 43. (Currently Amended) The bipolar transistor of
2 claim [[40]] 42, wherein
3 the silicide layer is a refractory metal silicide layer
4 of CoSi_2 or TiSi_2 .

1 44. (Previously Presented) The bipolar transistor of
2 claim 33, wherein
3 the extrinsic base region further has a poly-
4 crystalline portion over an oxide layer of the substrate.

1 45. (Previously Presented) The bipolar transistor of
2 claim 33, further comprising:
3 a silicide layer on a top surface of the extrinsic base
4 region to lower a contact resistance.

1 46. (Previously Presented) The bipolar transistor of
2 claim 45, wherein
3 the silicide layer is a refractory metal silicide layer
4 of CoSi_2 or TiSi_2 .

1 47. (Currently Amended) A bipolar transistor,
2 comprising:
3 a substrate having a mono-crystalline portion and an
4 oxide portion, the substrate to provide a collector region;
5 a plurality of epitaxial layers over the substrate,
6 each of the plurality of epitaxial layers having a mono-

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7 crystalline portion over the mono-crystalline portion of the
8 substrate and a poly-crystalline portion over the oxide
9 portion of the substrate; and
10 a polysilicon emitter on the mono-crystalline portion
11 of a first epitaxial layer of the plurality of epitaxial
12 layers;
13 wherein the plurality of epitaxial layers to provide a
14 raised extrinsic base located outside the polysilicon
15 emitter, the mono-crystalline portion of the first epitaxial
16 layer under the polysilicon emitter to provide an intrinsic
17 base, and the raised extrinsic base is thicker than the
18 intrinsic base.

1 48. (Cancelled)

1 49. (Previously Presented) The bipolar transistor of
2 claim 47, wherein
3 at least a second epitaxial layer of the plurality of
4 epitaxial layers is coupled to the first epitaxial layer to
5 provide the raised extrinsic base.

1 50. (Previously Presented) The bipolar transistor of
2 claim 49, wherein
3 the first epitaxial layer is a SiGe epitaxial layer and
4 the at least second epitaxial layer is a heavily p-type
5 doped Si or SiGe epitaxial layer.

1 51. (Previously Presented) The bipolar transistor of
2 claim 47, further comprising:

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3 a silicide layer on a top surface of the raised
4 extrinsic base to lower a contact resistance.

1 52. (Previously Presented) The bipolar transistor of
2 claim 51, wherein
3 the silicide layer is a refractory metal silicide layer
4 of CoSi_2 or TiSi_2 .

1 53. (Previously Presented) The bipolar transistor of
2 claim 47, wherein
3 the bipolar transistor is an npn transistor.

1 54. (Previously Presented) The bipolar transistor of
2 claim 53, wherein
3 the npn transistor is a Si, SiGe or SiGe:C npn bipolar
4 transistor.